

Design and performance of the front-end electronics of the LHCb Muon Detector

W. Bonivento (on behalf of the LHCb Muon Collaboration)

Istituto Nazionale di Fisica Nucleare – Sezione di Cagliari - Italy

Walter.Bonivento@cern.ch

Abstract

We present the architecture, design and prototype performance of the front-end electronics of the LHCb Muon System.

The design is finalised and the electronics boards are in a production phase.

I. SYSTEM ARCHITECTURE

The role of the LHCb Muon Detector is to detect muons tracks with high transverse momentum, as a signature of a B meson decay. This information is crucial for the first trigger level of the experiment, called level zero (LO) trigger.

The LHCb Muon Detector consists of 5 stations along the beam axis and is based on 3-GEM (Gas Electron Multiplier) detectors for the inner part of the first station and on MWPC (Multi-Wire Proportional Chamber) for the rest of the detector. The muon level zero trigger identifies a muon track looking for 5 hits (one per station) in coincidence within the same bunch crossing. There is a possible collision every 25 ns (the bunch crossing frequency is 40.08 MHz).

The trigger processor performs its algorithms on a binary space point information sent by the front-end electronics. About 126,000 channels are output from the detector, while the trigger processor receives only about 26,000 channels. Indeed, the granularity needed by the trigger is coarser than the granularity used on detector, which is constrained by the maximum channel capacitance allowed by the maximum tolerable channel noise levels.

II. FRONT-END REQUIREMENTS

The task of the wire chambers of the LHCb Muon System is to measure the arrival time of muons to better than 3 ns r.m.s. The chamber signal is characterized by a fast rising edge and a long $1/(t + 1.5 \text{ ns})$ tail, going over into a DC current lasting for about 20 μs . This signal has to be shaped to a unipolar narrow pulse in order to cope with the high rates expected in the experiment.

A detector gas gain of 10^5 together with an amplifier peaking time of 10 to 15 ns is found to be the optimum working point for this detector. This results in an average pulse height of about 60 fC of charge, when referred to a delta input signal. To obtain a narrow pulse, a tail cancellation circuit has to be implemented which should correctly work for at least 99 % of chamber signals (up to 250fC input charge), which sets the specification for the gain and linear range of the chip. In order to allow the desired threshold of 10 fC, the equivalent noise charge (ENC) at the input should not exceed 2 fC up to the largest detector capacitance of 250 pF. In addition, the

amplifier input impedance should be less than 50 ns to keep crosstalk low. High rates of up to 800 kHz per channel in some detector regions require fast pulse shaping and baseline restoration circuits to compensate for baseline shifts and fluctuations. A total accumulated dose of 1 MRad during the life of the experiment requires radiation tolerant chip technology.

III. THE FRONT-END BOARD

Chamber readout is organised such that two double (single) gaps are digitally OR-ed in the stations behind (before) the calorimeters. The front-end boards house three chips: two ASD chips, CARIOCA for the WPC and CARIOCAGEM for the triple-GEM detector, which perform the readout of the two double (single) gaps and a DIALOG chip which mainly perform the OR of the two ASD signals. Figure 1 shows the triple-GEM front-end board.

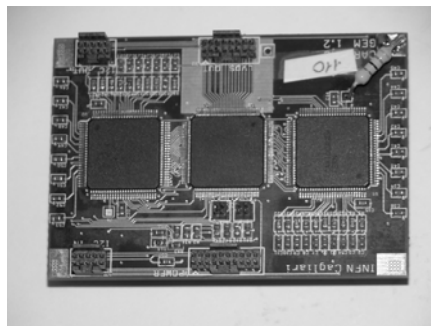


Figure 1: The triple-GEM detector front-end board

IV. THE CARIOCA AND CARIOCAGEM CHIP

A. Carioca

The CARIOCA integrated circuit is developed in two versions: one for cathode readout (positive input polarity version) and another for anode readout (negative input polarity version). Each chip is composed of eight identical channels and a bias network, that provides the bias voltages and currents to the channels. The block diagram of a single CARIOCA channel is shown in Figure 2.

The input of the CARIOCA circuit is pseudo-differential, consisting of two identical current-mode amplifiers. One amplifier is connected to the chamber pad through a trace on the printed circuit board (PCB). The other, dummy amplifier, has a floating input and it is used to provide DC balance to the shaper and common mode rejection to pickup, crosstalk and

noise on the power supply lines. Following the amplifier there is a shaper circuit and a differential amplifier which provide further gain together with signal and amplifier tail cancellation. The differential amplifier output is fed to the discriminator. The discriminator output is sent to the LVDS driver that provides the chip output signal.

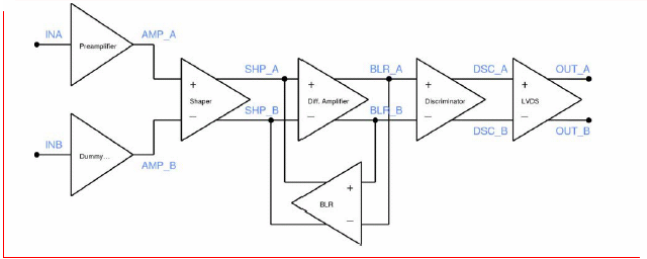


Figure 2: The triple-GEM detector front-end board

A baseline restoration circuit, realized as a nonlinear feedback loop around the second differential amplifier, limits baseline fluctuations.

The CARIOCA amplifier input stage is a cascode structure with a large input transistor, followed by a voltage to current converter and a current mirror. The input transistor ($N1$) is a n-channel with a length of $0.7 \mu\text{m}$ and width $1600 \mu\text{m}$, giving to an input capacitance of 6 pF . This transistor operates in moderate inversion and has 42 mA/V transconductance (g_m) at a drain current of about 3.2 mA . The folded transistor ($N2$) is chosen to have an open loop gain of about 30. The compensation capacitor (C_{feed}) of 406 fF is used to split the first two poles of the circuit and improve the stability. The designs of positive and negative polarity amplifiers, shown in Figure 3, are very similar and they have the same working principle.

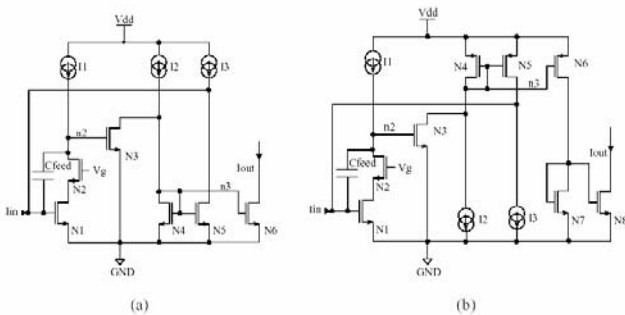


Figure 3: Simplified schematic of the CARIOCA amplifier for positive (a) and negative (b) input polarity.

The main difference is the output stage current mirror ($N5 / N6$). Since we want to have both amplifiers with the same output polarity, the current of the negative input polarity amplifier is inverted by an additional current mirror ($N7 / N8$). Current sources are realised with high impedance cascode transistors. A global bias circuit provides the required bias voltages for the circuit, setting the correct DC voltage level.

The positive amplifier has a gain of 3.0 mV/fC while the negative one has a gain of 2.7 mV/fC at an input capacitance of 60 pF . Considering the MWPC pad capacitance range (50 pF to 250 pF) the sensitivity decays from 3.2 mV/fC (2.8 mV/fC) to 2.1 mV/fC (1.6 mV/fC) and the peaking time increases from 7 ns (7 ns) to 14 ns (15 ns) for the positive (negative) input polarity amplifier.

The amplifier has a bandwidth of 22 MHz and 15 MHz for the positive and negative polarity amplifiers, respectively. Both amplifiers show a small signal gain around 30 dB . The input impedance is smaller than 50Ω for both amplifiers.

The shaper is a one stage pole/zero filter with 2 poles and 2 zeros. The input stage is a current-to-voltage converter. The output current from the amplifiers are converted into voltage by a $5 \text{ k}\Omega$ resistor and these voltages are sent to the shaper inputs. A simplified schematic of the shaper circuit is shown in Figure 4.

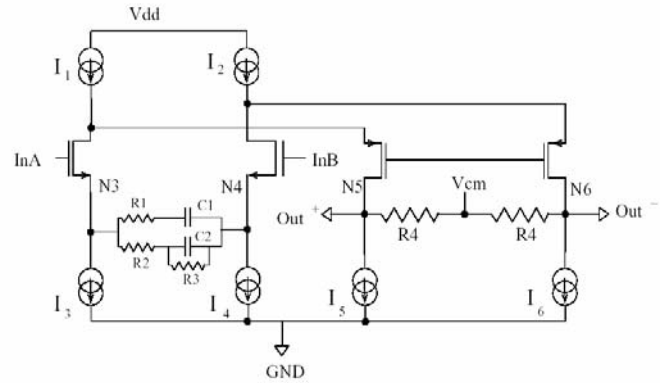


Figure 4: Simplified schematic of the shaper circuit

It consists of a differential amplifier in a folded cascode configuration with common-mode feedback. The DC output voltage is set by the common-mode voltage (V_{CM}) via $5 \text{ k}\Omega$ resistors.

The common-mode voltage is chosen to be 1.27 V to explore the maximum dynamic range of the signals.

The tail cancellation is performed by a double pole-zero compensation network.

The shaper gain is about 4.0 mV/fC and 3.6 mV/fC for the positive and negative polarity amplifiers, respectively.

The shaper circuit is designed with a speed such that the amplifier peaking time is not significantly degraded. The contribution to the peaking time is about 1 ns . Therefore the dominant high frequency pole is located at about 140 MHz . The shaper voltage gain peaks at about -37 dB in the range of 6 to 23 MHz .

The differential amplifier follows the basic design shown in Figure 5.

It serves as gain and shaping amplifier. The gain is set by the load impedance Z and the source impedance Y . The source impedance is a combination of resistors and capacitances, making a pole/zero structure to cancel the time constant of the amplifier output. Since the positive and negative input polarity amplifiers have a different tail, two different pole/zero

structures are chosen, i. e., the value of Y differs from positive to negative input polarity version.

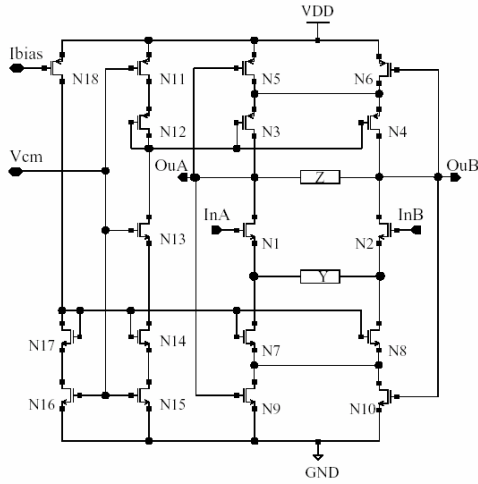


Figure 5: Differential amplifier schematic

The DC output voltage of the differential amplifier is established by common mode feedback. The output nodes are connected to the gates of N_5/N_6 and N_9/N_{10} , that operate in their linear region as resistors, with 100mV across N_5/N_6 and 62mV across N_9/N_{10} . Common mode gain is achieved by modulating the field effect transistor (FET) resistances via common mode output voltage. Common mode feedback drives the common mode output voltage to the reference voltage V_{cm} . This reference voltage is common to the differential amplifier and the baseline restoration circuit and is set to 1.5 V. The bias current (I_{bias}) is set by a bias network. The drain currents of the input pair N_1/N_2 is set by the mirrors N_{14} and N_{17} and it is a factor four higher than the bias current. The differential amplifier shows a linear voltage gain of 1.6 (6.3 m V/fC) and 2.0 (7.4 m V/fC) for the positive and negative input polarity, respectively, over the expected signal range.

The equivalent frequency spectrum of differential amplifier shows a gain of approximately -32dB (-28 dB) for the positive (negative) input polarity amplifier, in the range of 6 to 24 MHz with a -3 dB bandwidth of about 145 MHz

An active baseline restoration (BLR) is implemented in the CARIOCA chip.

This circuit, shown in Figure 6, consists of three amplifiers with the same structure of the one in Figure 5. The only difference is that the bias current mirror has a gain 1, which makes the input pair drain current equal to the bias current. The standing current in the first and third amplifiers ($BLR1$ and $BLR3$) is set by a polysilicon resistor R referred to the power supply, and not by I_{bias} . This current it is not fixed on the second amplifier ($BLR2$) because it has influence on the circuit time constant, as described below.

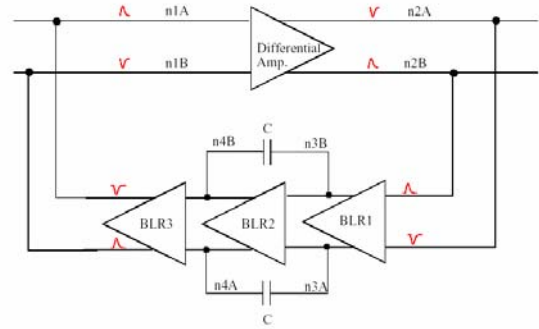


Figure 6: Schematic of the baseline restoration circuit

The baseline restorer transfer function is equal to a simple RC differentiating element and if all the stages would be linear in the entire signal range the BLR would just differentiate the signal resulting in a bipolar signal shape. The essential feature of the BLR is that the first stage is nonlinear i.e. the signal is clipped at a design value of 50 mV. Therefore only small signals enter the feedback which provides the desired baseline restoration.

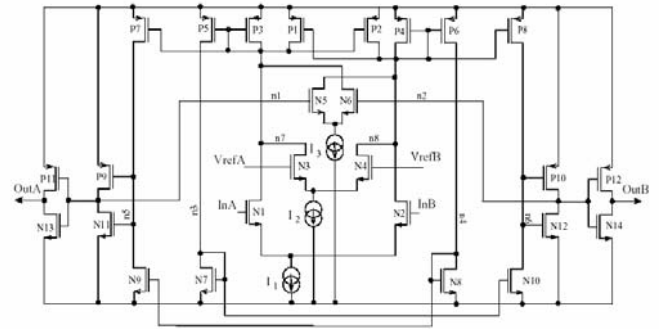


Figure 7: Schematic of the discriminator circuit

The discriminator, whose design is based on an existing circuit, is a high-gain differential amplifier with symmetric current-mirror loads. Figure 7 shows the schematic. The threshold voltage is set in a differential way on the nodes V_{refA} and V_{refB} and these voltages unbalance the current through the main differential pair. The amount of hysteresis is programmable by means of a current source (I_3), which shifts the effective discriminator threshold. The bias currents I_1 , I_2 and I_3 are supplied from an external input through current mirrors.

The discriminator gain peaks at -84 dB in the range from 7 to 13 MHz

B. Carioca-GEM

The triple-GEM signal is very different from that of wire chambers and it is possible to approximate it to a current pulse of 10 ns risetime, a 20ns flat top and a 10ns fall time. For the readout of this signal the shaping circuit of the CARIOCA had to be modified, removing the ion tail cancellation circuit, and therefore a new chip was designed. Figure 8 shows the delta response of both CARIOCA and CARIOCAGEM circuit.

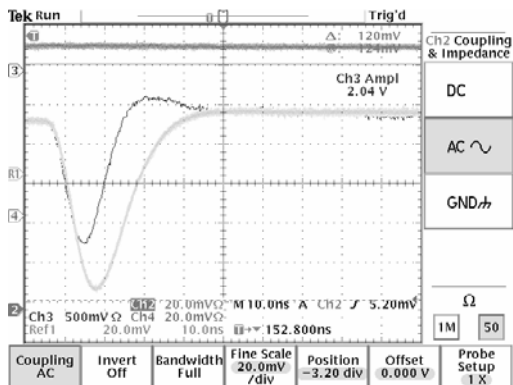


Figure 8: Delta response of both CARIOCA (dark line) and CARIOCAGEM circuit.

V. THE DIALOG CHIP

DIALOG (DIagnostic, time Adjustment and LOGics) is a custom integrated circuit. The reduction from the 126,000 front-end channels (which are called *Physical Channels*) to the 26,000 trigger channels (called *Logical Channels*) is performed as soon as possible in order to minimize the number of signal connections.

The first goal in designing DIALOG is to realize channel reduction already at the front-end level. The logic function to be used in channel reduction depends on the channel position inside the detector, therefore DIALOG must be configurable to allow different possible combinations. Another key task for the circuit is to make it possible proper detector time alignment channel by channel, which is also necessary for a correct operation of the muon trigger. It also performs threshold levels generation for the front-end chip, front-end monitoring facilities dedicated to system debug and diagnostics.

DIALOG is developed in CMOS IBM 0.25 μm technology. The choice of an ASIC is due to the following two reasons.

- 1) The radiation dose on detector approaches 1Mrad. This already excludes the use of commercial circuits.
- 2) Bearing in mind the detector structure and performance, it is also important to minimize the CARDIAC connections and size while implementing the full set of functionalities needed by the system.

The CARIOCA chip has eight binary outputs, hence DIALOG manages a total of 16 Physical Channels, while a maximum of 8 Logical Channels are output.

The DIALOG block diagram is shown in Fig. 9. Following the processing stages from input to output different functional blocks can be identified:

- the input block (16 differential pairs);
- the programmable delayer and digital shaper blocks, one per channel;
- the masking block;
- the logical channels generation units.

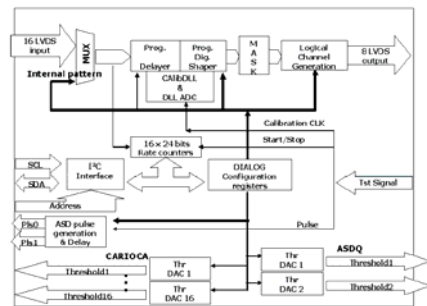


Figure 9: DIALOG internal scheme

Each single input channel can be delayed by 0 to 31 programmable steps. Each step adds a delay of about 1.6 ns provided by a Voltage Controlled Delay Line. All input channels are reshaped in width using a programmable digital shaper. A mask is foreseen for the selection (or deselection) of each input channel. This allows for:

- 1) direct access to the Physical Channels, even after the logic combination to generate the Logical Channel is set;
- 2) possibly masking noisy or defective front-end channels.

The specific logic function used to generate the Logical Channels is written on dedicated registers accessed by the I²C bus interface. The possible logic combinations are:

- logic OR of 2, 4 or 8 input channels
- logic OR of 2 (4) signals that are the logic AND of 2input channels.

All DIALOG facilities are configured by the I²C interface and the control data are stored inside 93 8-bit registers. Each DIALOG has a 7-bit address, however 3 of these are fixed and the longest I²C chain contains 16 DIALOG circuits.

DIALOG provides 18 independent threshold signals for the ASD discriminators, using an integrated 8-bit DAC (Digital to Analog Converter) and a linear output driver for each threshold level.

DIALOG tools used for system control and diagnostics are the following:

1. It is possible to generate an internal pattern to test the DIALOG data acquisition chain. The pattern is multiplexed at the DIALOG input with signals coming from the CARIOCA chips
2. . Input signals can be sent to rate counters for monitoring purposes. There are sixteen 24-bit rate counters to monitor the front-end rate and noise.
3. . DIALOG outputs two independent pulse signals to test the CARIOCA chips.

VI. CHAMBER TESTS

Chamber tests of the front-end boards were performed on both MWPC and triple-GEM detectors. The tests have shown that it is possible to obtain the desired time and space resolutions with the various detector types. As an example performance Figure 10 shows the average output pulse width form the

CARIOCA chip with a WPC chamber with an Am(241) radioactive source.

Figure 11 shows the average pulse shape from the triple-GEM chamber with an Am(241) radioactive source.

In both cases it is seen that the circuit behaves correctly as far as pulse shaping is concerned.

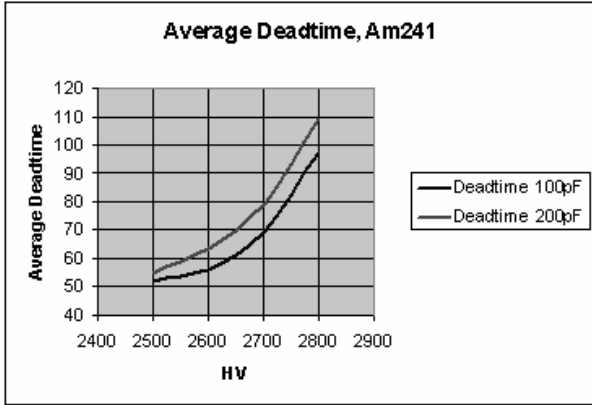


Figure 10: Output Pulse width from the CARIOCA chip with a WPC chamber with an Am(241) radioactive source

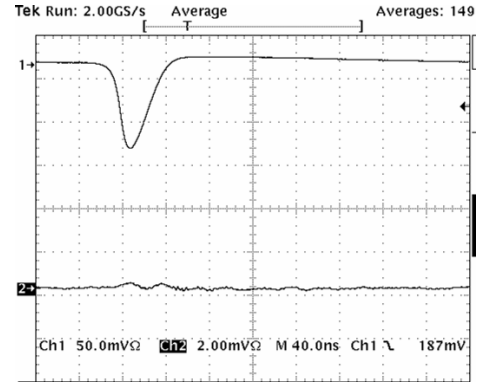


Figure 11: Average analog output pulse from the triple-GEM chamber with an Am(241) radioactive source

VII. REFERENCES